REMARKS

Claim 9 was rejected as anticipated by FELDMAN 6,781,445. Reconsideration and withdrawal of the rejection are respectfully requested.

FELDMAN does not disclose the logic circuit that develops first and second sinusoidal signals whose phases differ by 180°. The Official Action states that the reference discloses a logic circuit that develops the signals VIN+ and VIN- that are sinusoidal signals whose phases differ by 180°. However, VIN+ and VIN- are input voltages (column 3, line 8). The reference does not disclose how these input voltages are developed or that they are developed by a logic circuit. Indeed, the reference does not disclose any circuitry for developing these input voltages. The development of these signals is unknown and therefore speculative. A rejection cannot be supported by speculation and claim 9 therefore avoids the rejection under §102.

Claims 1-2 and 5-8 were rejected as unpatentable over KAWASHIMA 5,699,305 in view of ONODERA et al. 5,121,284. Reconsideration and withdrawal of the rejection are respectfully requested.

With regard to claims 1-2, KAWASHIMA discloses an amplifier circuit that receives first and second inputs (n1, n2) and develops first and second outputs (n3, n4). The Official Action points to transistors 66 and 67 as corresponding to the

claimed first and second P-channel transistors. However, the gates of transistors 66 and 67 are connected to the first and second outputs, not to the first and second inputs as claimed. This is a significant difference because the connection of the transistors to the outputs rather than the inputs means that the circuit will operate differently, if at all.

Further, ONODERA et al. do not provide any motivation to add a resistor element connected between the first and second outputs. ONODERA et al. disclose a driver circuit connected to an inductive load, where the inductive load is represented in Figure 3 by the equivalent circuit 20 that includes an inductor and a resistor. In other words, the inductor and resistor merely represent the inductive load that is attached to the outputs from the driver circuit. There is nothing in the reference that motivates one of skill in the art to actually add a resistor between the outputs. The Official Action states that the motivation to add the resistor is to provide a desired output impedance to drive a subsequent circuit. ONODERA et al. do not state this; the only place that this motivation is found is in the present application. The equivalent circuit 20 is the "subsequent circuit" being driven and thus the appearance of an equivalent resistor is not a motivation to change an output impedance.

The same argument applies to the inductive element of claim 2. The equivalent inductor disclosed in ONODERA et al. is

no motivation to add an inductive element between the outputs. Further, claim 2 provides that the resistive and inductive elements are connected in series; ONODERA et al. disclose a parallel connection.

Accordingly, neither reference discloses the claimed first and second P-channel transistors and there is no motivation to modify KAWASHIMA to include the claimed resistive and inductive elements, and thus claims 1-2 avoid the rejection under §103.

Claims 5-8 include an inductive element and the Official Action points to ONODERA et al. for the suggestion to modify KAWASHIMA to include this feature. As explained above, ONODERA et al. disclose an equivalent inductor in an equivalent circuit representing the inductive load and does not motivate the artisan to add an inductive element. Accordingly, claims 5-8 avoid the rejection under §103 for the same reason as given above.

Claims 6 and 8 are also allowable because, as explained above, the gates of transistors 66 and 67 in KAWASHIMA are connected to the first and second outputs, not to the first and second inputs as claimed in claims 6 and 8.

Claims 3-4 were rejected as unpatentable over KAWASHIMA in view of ONODERA et al. and LLEWELLYN 6,724,248. Reconsideration and withdrawal of the rejection are respectfully requested for reasons given above for claims 1-2. As best

understood, the Official Action indicates that it would be obvious to try various arrangements of inductors and resistors, and that this makes the specific arrangements of resistive and inductive elements claims 3-4 obvious to one of skill in the art. It is well established that obvious-to-try is not an acceptable standard for rejecting a claim under §103 and thus these claims further avoid the rejection under §103.

Claim 10 was rejected as unpatentable over FELDMAN. Reconsideration and withdrawal of the rejection are respectfully requested. This claim is allowable for the reasons given above for claim 9, from which claim 10 depends. Further, FELDMAN discloses that the gates of the first and second N-channel transistors are connected to a bias voltage, while the sources of the first and second P-channel transistors are connected to VDD. Thus, the sources of the first and second P-channel transistors do not receive "said power supply potential" as is called for in the claim. In addition, the gates of the first and second P-channel transistors are connected to the first and second outputs, not the first and second inputs as claimed. Accordingly, FELDMAN does not disclose or suggest the subject matter of claim 10, which avoids the rejection under §103.

Claims 11-13 were rejected as unpatentable over KAWASHIMA in view of ONODERA et al. and FUKUI 6,114,906. Reconsideration and withdrawal of the rejection are respectfully

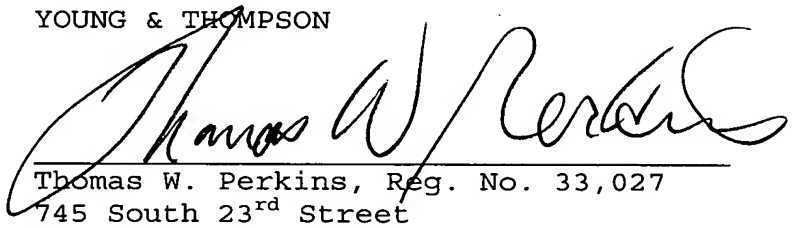
requested for the same reasons as given for allowance of claims 1-2.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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